REMARKS

The Final Office Action mailed December 17, 2009, has been received and carefully noted. Claims 1-9 and 11-29 are currently pending in the subject application and are presently under consideration. Claims 1, 3, 5, 7, 15-18 are amended. Claims 19 and 23-29 are canceled. Support for the amendments can be found in at least paragraph [0017], [0023]-[0025] and figures 1-3 of the Specification.

Favorable reconsideration of the pending claims is respectfully requested in view of the amendments and the following comments.

Examiner Interview

An Examiner Interview was conducted on May 6, 2010, including Examiner Corey S. Faherty, Farzad Amini, and Kim Leung. In the Examiner Interview, the possibility of amending the claims to recite additional elements regarding the operation of the claimed processor was discussed. In response, the claims are amended to include additional limitations that are disclosed in the Specification.

Claim Rejections Under 35 U.S.C. §102

Claims 1-7, 9, and 11-16 are rejected under 35 U.S.C. §102(b) as being anticipated by Gove (U.S. Patent No. 5,613,146) ("Gove"). The Applicants respectfully request reconsideration and withdrawal of these rejections because the claims as amended are not anticipated by Gove.

Amended independent claim 1 recites, among other elements, *configuring, by the external host controller, a data path through a mesh arrangement of data ports for transferring data between a second processing unit of the data driven processor and external memory* and *the mesh arrangement of data ports allows data flow from any one of the processing units directly to another without accessing memory*. These elements of claim 1 are not anticipated by Gove.

The Examiner alleges that Gove anticipates *configuring, by the external host controller, a data path*, citing FIG. 52 and its accompanying description or column 13 lines 25-42 of Gove. See Office Action mailed December 17, 2009, page 3. However, Gove does not appear to

disclose this element of claim 1. Rather, the figure and sections cited by the Examiner states that "a host 5205 . . . provides necessary image information . . . to the image system processor 5200" and that the "master processor . . . is used for . . . control of the entire system, including the control of the transfer processor as well as the interaction between the various processors" and "can control the type of data and the manner in which the data is obtained by the transfer processor." Accordingly, the host processor disclosed in Gove only provides image information to Gove's system and does not have the ability to configure communication of data between the processors. Furthermore, the master processor is an internal component of Gove's system rather than an external controller as recited by claim 1.

Additionally, Gove does not appear to disclose *the mesh arrangement of data ports allows data flow from any one of the processing units directly to another without accessing memory*. Rather, Gove discloses a system where multiple processors are interconnected with multiple memories by a crossbar switch for the interchange of data. See Gove, column 3 lines 1-3. The global data ports and local data ports of the processing units in Gove may only access the crossbar switched memories. See Gove, column 36 lines 25-38, column 39 lines 1-13, FIG. 30. When one processor needs to transmit data to any other processor, the processor places the data in memory to be read by the other processors. The processor placing the data in memory then signals selected other processors, via an interrupt bus, that data is waiting in memory. The crossbar switch then connects the signaled processors to the memory where the data is located. The signaled processors then read the data from memory. See Gove, column 3 lines 8-20, column 8 lines 2-10, column 10 lines 26-47, column 12 lines 5-19, column 13 lines 1-13, column 37 lines 9-13, column 52 lines 37-42, column 54 lines 11-13, column 58 lines 17-29, column 61 lines 26-40. In other words, the data ports of the processors in Gove are not connected for direct communication of data. Each processor must access memory to transfer data between them. In contrast, the Applicants' claim 1 allows for *data flow from any one of the processing units directly to another without accessing memory*.

For at least the reasons mentioned above, Gove fails to disclose the above elements of Applicants' claim 1 and thus does not anticipate claim 1. Therefore, reconsideration and withdrawal of the rejection of claim 1 based on 35 U.S.C. §102(b) are requested.

Independent claim 5 includes some elements analogous to those discussed above in regard to claim 1 including *the data ports of adjacent processing units being coupled to each other in a mesh arrangement of point-to-point connections and programmable to allow data flow from any one of the processing units directly to another without accessing memory* and *a host interface unit to receive instructions, from an external host controller, that configure the data flow between the data ports of adjacent processing units and between the data ports and the DMA unit to create a data path from one of the processing units to external memory*. For at least the reasons mentioned above in regard to claim 1, claim 5 is not anticipated by Gove.

Claim Rejections Under 35 U.S.C. §103

Claims 8 and 17-22 are rejected under 35 U.S.C. §103(a) as being obvious over Gove. The Applicants respectfully request withdrawal of these rejections because these claims are not obvious in view of Gove.

Independent claim 17 includes some elements analogous to those discussed above in regard to claim 1 including *an external host controller, the data ports of adjacent processing units being coupled together in a mesh arrangement of point-to-point connections and programmable to allow data flow from any one of the processing units directly to another without accessing memory*, and *a host interface unit to receive instructions from the external host controller that configure the data flow between the data ports of adjacent processing units and between the data ports and the memory access unit to create a data path from one of the processing units through the mesh arrangement of data ports to the external memory*. For at least the reasons mentioned above in regard to claim 1, claim 17 is not obvious over Gove.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. The Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: May 10, 2010.

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I hereby certify that this paper is being transmitted online via EFS Web to the Patent and Trademark Office, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on May 10, 2010.

Margaux Rodriguez *May 10, 2010*